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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/696,651	10/30/2003	Vincent Cedric Colnot	P1985	7795	
24739 7590 10728/2008 CENTRAL COAST PATENT AGENCY, INC 3 HANGAR WAY SUITE D			EXAM	EXAMINER	
			SUN, SCOTT C		
WATSONVIL	LE, CA 95076		ART UNIT	PAPER NUMBER	
			2182		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) 10/696.651 COLNOT, VINCENT CEDRIC Office Action Summary Examiner Art Unit SCOTT SUN 2182 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 06 October 2008. 2a) ☐ This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-11.13-25.27 and 28 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) _____ is/are allowed. 6) Claim(s) 1-11,13-25,27 and 28 is/are rejected. 7) Claim(s) _____ is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are; a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abevance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)

Notice of Draftsperson's Patent Drawing Review (PTO-948)

Information Disclosure Statement(s) (PTO/S5/08)
 Paper No(s)/Mail Date ______.

Paper No(s)/Mail Date.

6) Other:

5) Notice of Informal Patent Application

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/6/2008 has been entered.

Response to Arguments

- Applicant's arguments filed 106/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:
 - a. Prior art of record does not teach an "on-chip" oscillator.
 - b. Prior art of record does not teach "a single connection port"
- 3. In response to argument 'a', examiner notes that the cited portions of prior art, Atsmon, are directed to a <u>processor</u> (PIC 16F84), and therefore on-chip clearly means on the processor chip. However, the memory card itself contains a layer of silicon on which the processor and other circuits are printed. Therefore, while the oscillator is not on the processor, it is still on the silicon portion of the memory card, which is interpreted as on-chip. Likewise, there is no mention that applicant's oscillator is on the processor portion of the memory card, but merely that the oscillator is on-chip, or "circuitry of which is contained in the secure memory device" as claimed.

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- 4. Examiner further notes that the actual uses cited by the applicant of the modem interface (FSK and PSK) are not cited in the claims, and therefore cannot be relied upon to exclude uses of the oscillator. It is reminded that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.
 See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
- 5. In response to argument 'b', examiner notes that the single connection port in the prior art is the port which the multiple interfaces use to communicate with the processor. It is clear that all the interfaces (ISO, USB, wireless) all are converged into a single interface for the processor as shown in the rejection. While prior art might not explicitly state this, it is implied in the drawing and the cited portions of the prior art. If all three interfaces did not share the single connection port into the processor, then why does the prior art does show three separate ports into the processor? Furthermore, why would it be necessary to convert these three types of data?

Examiner further notes that the claim does not specify the communication counterparts of the connection port. In other words, the claim does not specify that the single connection port communicates with two different interfaces of the host, and therefore does not preclude that the single connection port is used to communicate data between the internal processor and three cited interfaces.

Having responded to each of applicant's arguments, examiner notes that prior art
of record still provides a valid ground of rejection, as attached below.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this identification of the invention of the subject matter sould be able that are such that the subject matter sould be able to the subject matter sould be able to the subject matter sould be an advantage of the subject matter sould be able to the subject matter of the

- Claims 1, 2, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsmon et al (US Patent #6,607,136) in view of Leydier et al (PG Pub #US 2003/0046554 A1)
- Regarding claim 15, Atsmon discloses a secure memory device (system shown in figure 1) for use with and contained within a smart card with a modern interface comprising circuitry of:

A rewritable memory (memory unit 22, figure 2; column 12, lines 38-42);

A processing unit or a microprocessor (processing unit 21);

An on-chip oscillator (oscillator circuit or RC circuit; column 13, lines 4-11), circuitry of which is contained in the secure memory device; examiner notes that Atsmon teaches both circuits being external. However, both circuits are external to the processor, not to the card. This is evidenced by the fact that Atsmon teaches the type of oscillator used is limited by the size of the card. Atsmon also teaches that the oscillator would be connected to the OSC1/CLKIN pin of the processor (figure 7). Accordingly, examiner asserts that the oscillator is on-chip (on the card).

An ISO 7816 interface (column 25, lines 12, 13);

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A one-wire modem interface (transducer; column 11, lines 37-39);

Characterized in that both communication interfaces are bidirectional (input/output unit 35, figure 3; column 11, lines 36-40); Examiner notes that the I/O unit 35 can both receive and transmit data (therefore bi-directional).

Atsmon does not disclose explicitly that both communication interfaces share the same I/O terminal. However, Leydier discloses a smartcard (figure 13) such that communication interfaces (ISO, USB, Wireless ports) share a single I/O terminal (communication interface 190, paragraph 59) providing a single connection port on the secure memory device for both of the communication devices (figure 13, connection port to processor 169). Teachings of Atsmon and Leydier are from the same field of smartcards, and specifically of multiple communication interface smartcards.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Atsmon and Leydier by using a common I/O terminal in the smartcard system of Atsmon for the benefit of converting data between different protocols (paragraph 59).

10. Regarding claim 2, Atsmon further discloses a secure memory of device as in claim 1, exchanging data with a host in the form of a modulated signal by means of a card reader reading the smart card (air, column 15, line 7), the smart card characterized by possessing all processing means required for exchanging data with the card reader (examiner notes that both Atsmon and Leydier teaches that the medium of transmission could be air, i.e. wireless transmission of acoustic signals).

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 Claims 3-11, 13, 14, 17-25, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsmon and Leydier further in view of Saitoh (US Patent # 5,929,414).

12. Regarding claim 3, Atsmon and Leydier combined discloses claim 2, but does not disclose explicitly when a reset input that controls activation of ISO interface and modem interface. However, Saitoh discloses a memory device (figure 1) wherein an ISO interface (contact 55) is active when a reset input is high, and a modem interface (modem 57) is active when the reset input is low (column 5, lines 22-43; lines 59-65). Examiner notes that Saitoh discloses the modem being activated and connected to the CPU when VCC from a contact reader/writer is off. This means that reset input is also low (off) because a contact reader/writer provides a reset ON only when VCC is on.

Teachings of Atsmon, Leydier and Saitoh are from the same field of IC cards, and specifically of communication interface design of IC cards. Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to combine teachings of Atsmon, Leydier and Saitoh by using the selector circuitry and logic in the combined IC card system for the benefit of switching between contact and contact-less data transfer in one IC card (column 2, lines 35-38).

13. Regarding claim 4, Atsmon, Leydier and Saitoh combined disclose claim 3, where Saitoh further discloses transmitting a modulated answer to reset to the host when the reset intput is pulled down (column 3, lines 65-68; column 4, lines 1-2).
Examiner notes that modem (contact-less interface to reader/writer) also conforms to ISO 7816-3, and therefore must communicate with the reader/writer in the same format.

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This is further evidence by Saitoh's teachings of a reader/writer that communicates with either contact or contactless IC cards (column 8, lines 29-40).

- 14. Regarding claim 5, Atsmon, Leydier and Saitoh combined disclose claim 4, where Saitoh further discloses transmitting the MAR only once, when the card is inserted into the card reader (column 8, lines 29-51). Examiner notes this operation is also defined by ISO standard 7816.
- 15. Regarding claim 6, Atsmon, Leydier and Saitoh combined disclose claim 5, where Saitoh further discloses where the MAR comprises at least three fields, a header, a card number and a random number. Examiner notes these fields are according to ISO standard 7816.
- 16. Regarding claim 7, Atsmon, Leydier and Saitoh combined disclose claim 6, where Saitoh further discloses computing a new random number prior to transmit the MAR. Examiner notes this again is a requirement of ISO standard 7816.
- 17. Regarding claim 8, Atsmon, Leydier and Saitoh combined disclose claim 3, where Atsmon further discloses transmitting data to and receiving data from a PC by means of a card reader plugged into the microphone input and the speaker output of the PC sound card (figure 1; column 31, lines 29-52).
- 18. Regarding claim 9, Atsmon, Leydier and Saitoh combined disclose claim 8, but does not disclose explicitly powered by voltage provided by the microphone input of the sound card. Examiner asserts that it would have been obvious for a person of ordinary skill in the art at the time of invention to provide power to the card using the a source on

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9).

the host or card reader because it would eliminate need of a power source on the card, which is further evidenced by teachings of Leydier (paragraph 60).

- 19. Regarding claim 10, Atsmon, Leydier and Saitoh combined disclose claim 3, and Atsmon further discloses transmitting data to and receiving data from an IVR server by means of a card reader plugged into the telephone line (column 10, lines 60-65; column 20, lines 1-18).
- 20. Regarding claim 11, Atsmon, Leydier and Saitoh combined disclose claim 10, but does not disclose explicitly powered by voltage provided by the telephone line.
 Examiner asserts that it would have been obvious for a person of ordinary skill in the art at the time of invention to provide power to the card using the telephone line because it would eliminate the need of a power source on the card (also see the rejection of claim
- 21. Regarding claim 13, Atsmon, Leydier and Saitoh combined disclose claim 2, but does not disclose explicitly powered by a battery cell within the card reader. Examiner asserts that it would have been obvious for a person of ordinary skill in the art at the time of invention to provide power to the card using battery cell within the card reader because it would eliminate the need of a power source on the card (also see the rejection of claim 9).
- Regarding claim 14, Atsmon, Leydier and Saitoh combined disclose claim 3,
 where Saitoh further discloses where Vcc is connected to an ISO contact C1, Rst to an
 ISO contact C2, Clk to an ISO contact C3, Gnd to an ISO contact c5, and I/O to an ISO

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contact C7. Examiner notes that these connections are all part of the ISO 7816 standard.

 Claims 17-25, 27, 28 are substantially similar to claim 3-14. The same rejection is applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT SUN whose telephone number is (571)272-2675. The examiner can normally be reached on Mon-Thu, 10:00am-8pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Tariq Hafiz/ Supervisory Patent Examiner, Art Unit 2182